Amendments to the Specification:

Please amend the specification as follows:

Page 20, lines 18- 25, replace with the following:

As shown in Fig. 5, by applying a voltage obtained by connecting the boosting capacitor 311 and the boosting capacitor 312 to the electricity-generating unit 101 in series to the storage capacitor 313, the storage capacitor 313 is charged. As a result, the ~~boosting~~ storage capacitor 313 is charged up to a voltage of four times the open voltage of the electricity-generating unit 101. That is, when the open voltage of the generation voltage is 0.4 voltage, boosting is performed up to 1.6 voltage.

Page 34, lines 9-11, replace with the following:

The fifth AND gate 719 is a two-input AND gate, and outputs a logical product of a backup signal Sj and ~~the first NAND gate 711~~ an output of the first NAND gate 711. An output of the fifth AND gate 719 is a third charging-switch signal Sh.

Page 49, lines 5-10, replace with the following:

The frequency-dividing circuit ~~801~~ 1801 outputs a boosting signal Sd and a charging clock Se. On the other hand, the frequency-dividing circuit 1801 does not output, to the control-signal generating unit 1802, a pulse signal with 1 hertz and a pulse signal with 2 hertz for generating a backup original signal Sc that serves as a reference for a boosting behavior.